

inputted via said connector; and

an address control logic circuit for managing addresses for the plurality of logic blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions are simultaneously busy, exists. --

#### REMARKS

Claim 63 is amended.

Claims 64-65 are added.

Claims 63-65 are currently pending in this application.

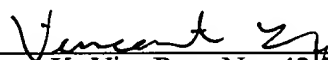
By this Preliminary Amendment, claim 63 is being amended to clarify the scope of the present application. Claim 64 is being added to further define the cells in each physical block of the flash memory partitions so that each cell of the flash memory can be individually programmable into more than two states in order to store more than one bit of data per cell. In addition, Claim 65 is being added to further define the cells in each physical block of the flash memory partitions so that each cell of the flash memory can be individually programmable into two states in order to store one bit of data per cell. These additional limitations of the flash memory cells are fully disclosed in the U.S. patent no. 5,095,344, filed on June 8, 1988, and U.S. patent application Serial No. 07/337,579, filed April 13, 1989, now abandoned, and these two documents are both incorporated by reference on page 11 of the specification of the present application.

Please note that claims 63-65 of the present application are substantial copy of claim 1 of U.S. patent no. 5,648,929 - Miyamoto et al. (1997). A copy of this patent has been filed herewith with the original application.

A prompt examination and allowance of the present application is solicited.

Dated: 12/23/98

Respectfully submitted,

  
\_\_\_\_\_  
Vincent K. Yip, Reg. No. 42/245  
MAJESTIC, PARSONS, SIEBERT & HSUE PC  
Four Embarcadero Center, Suite 1100  
San Francisco, CA 94111-4106  
Telephone: (415) 248-5500  
Facsimile: (415) 362-5418

Atty. Docket: HARI.006USQ